2004 International Conference on Computing Frontiers – CF'04
Technical Program
Wednesday, 14 April 2004

08:00AM Registration

09:00AM Opening Remarks

Chair: Stamatis Vassiliadis (Delft University of Technology, The Netherlands)

09:10AM Keynote Address

Chair: Gearold Johnson (Colorado State University, USA)

Quantum Parallelism and the Exact Simulation of Physical Systems	Dan C. Marinescu (University of Central Florida, USA)

10:10AM Session 1: Software Environments

Chair: Renzo Davoli (University of Bologna, Italy)

JSetL: Declarative Programming in Java with Sets	G. Rossi and E. Poleo (University of Parma, Italy)
Effect of Auto-tuning with User's Knowledge for Numerical Software	T. Katagiri, K. Kise, H. Honda and T. Yuba (The University of Electro-Communications, Japan)

11:00AM Coffee break

11:20AM Session 2: Special Session on NOMADS (Networks of Mobile Adaptive Dependable Systems)

Organizer and Chair: Miroslaw Malek (Humboldt-University of Berlin, Germany)

Introduction to NOMADS (Networks of Mobile Adaptive Dependable Systems)	M. Malek (Humboldt-University of Berlin, Germany)
An Architectural Framework and a Middleware for Cooperating Smart Component	A. Casimiro (University of Lisbon, Portugal), J. Kaiser (University of Ulm, Germany) and P. Verissimo (University of Lisbon, Portugal)
An Architecture to Support Cooperating Mobile Embedded Systems	E. Nett and S. Schemmer (University of Magdeburg, Germany)
Model-based Evaluation of a Radio Resource Management System for Wireless Networks	S. Porcarelli, F. Di Giandomenico (CNR, Italy), A. Bondavalli (University of Florence, Italy) and P. Lollini (University of Florence, Italy)

01:00PM Lunch

02:10PM Session 3: Pervasive Computing

Chair: Manfred Glesner (Darmstadt University of Technology, Germany)

Modeling Service-Based Multimedia Content Adaptation in Pervasive Computing	G. Berhe, L. Brunie and J.-M. Pierson (INSA de Lyon, France)
A Framework for Resource Discovery in Pervasive Computing for Mobile Aware Task Execution	K.Kalapriya, S.K.Nandy, D. Srinivasan, R.U. Maheshwari and V. Satish (Indian Institute of Science, India)
Application-Level Power Management in Pervasive Computing Systems: a Case Study	L. Negri, D. Barretta and W. Fornaciari (Politecnico of Milan, Italy)

03:25PM Session 4: Quantum Computing

Chair: Massimo Palma (University of Milan, Italy)

Quantum Designer and Network Simulator	S. Imre, P. Abronits and D. Darabos (Budapest University of Technology and Economics, Hungary)
Using HDLs for Describing Quantum Circuits: a Framework for Efficient Quantum Algorithm Simulation	M. Udrescu, L. Prodan and M. Vlădutiu ("Politehnica" University, Romania)
Toward a Quantum Process Algebra	P. Jorrand and M. Lalire (IMAG, France)

04:40PM Coffee break

05:00PM Session 5: Computational Models

Chair: Nader Bagherzadeh (University of California at Irvine, USA)

States of Matter, Information Organization and Dimensions of Expressiveness	M. Ceruti (Space and Naval Warfare Systems Center, USA)
BLOB Computing	F. Gruau, Y. Lhuillier (Paris South University & INRIA Futurs, France), P. Reitz (Montpellier University, France) and O. Temam (Paris South University & INRIA Futurs, France)
Biologically Inspired Rule-Based Multiset Programming Paradigm for Soft-Computing	E.V. Krishnamurthy (Australian National University, Australia), V.K. Murthy (University of New South Wales, Australia) and V. Krishnamurthy (University of British Columbia, Canada)
Watson-Crick Automata and PCFAS with Two Components - A Computational Power Analogy	L. Cojocaru (Rovira i Virgili University of Tarragona, Spain)

06:40PM End of sessions

Thursday, 15 April 2004

08:00AM Registration

08:30AM Session 6: Special Session on Memory Wall

Organizer and Chair: Mateo Valero (Technical University of Catalonia, Spain)

Reflections on the Memory Wall	S. A. McKee (Cornell University, USA)
Fighting the Memory Wall with Assisted Execution	M. Dubois (University of Southern California, USA)
Self-Correcting LRU Replacement Policies	M. Kampe, P. Stenstrom (Chalmers University of Technology, Sweden) and M. Dubois (University of Southern California, USA)
Dynamic Techniques to Reduce Memory Traffic in Embedded Systems	B. Juurlink and P.J. de Langen (Delft University of Technology, The Netherlands)
Overcoming the "Memory Wall" by Improved System Design Exploration and a Link to Process Technology Options	A. Papanikolaou, M. Miranda (IMEC, France) and F. Catthoor (IMEC & Catholic University at Leuven, France)
A First Glance at Kilo-instruction Based Multiprocessors	M. Galluzzi (Technical University of Catalonia, Spain), V. Puente (Cantabria University, Spain), A. Cristal (Technical University of Catalonia, Spain), R. Beivide, J.A. Gregorio (Cantabria University, Spain) and M. Valero (Technical University of Catalonia, Spain)

11:00AM Coffee break

11:20AM Session 7: Cache

Chair: Michel Dubois (University of Southern California, USA)

An Active Data-aware Cache Consistency Protocol for Highly-Scalable Data-Shipping DBMS Architectures	K. Wu, P.-f. Chuang and D.J. Lilja (University of Minnesota, USA)
Reducing Traffic Generated by Conflict Misses in Caches	P.J. de Langen and B. Juurlink (Delft University of Technology, The Netherlands)

12:10PM Session 8: Power Awareness

Chair: Cecilia Metra (University of Bologna, Italy)

Combining Compiler and Runtime IPC Predictions to Reduce Energy in Next Generation Architectures	S. Chheda (BlueRISC Inc., USA), O. Unsal (Intel Research Center, Spain), I. Koren, C.M. Krishna and C.A. Moritz (University of Massachusetts at Amherst, USA)
A Docked-Aware Storage Architecture for Mobile Computing	C.R. LaRosa and M.W. Bailey (Hamilton College, USA)

01:00PM Lunch

02:10PM Session 9: Networks

Chair: Fabrizio Lombardi (Northeastern University, USA)

Knowledge-Based Generic Intelligent Network Model	Gábor Németh (Technical University of Budapest, Hungary)
An Information-Interconnectivity-Based Retrieval Method for Network Attached Storage	Iliya Georgiev (Metro State College of Denver, USA)
Improving the Execution Time of Global Communication Operations	M. Kühnemann (Technical University Chemnitz, Germany), T. Rauber (University of Bayreuth, Germany) and G. Rünger (Technical University Chemnitz, Germany)
Mobile Agent-Based Module Distribution in Heterogeneous Networks	A. Wagner (Budapest University of Technology and Economics, Hungary)

03:50PM Session 10: Clusters

Chair: Gábor Németh (Technical University of Budapest, Hungary)

Berserkr: a Virtual Beowulf Cluster for Fast Prototyping and Teaching	M. Spigarolo and R. Davoli (University of Bologna, Italy)
A Parallel Backtracking Framework (BkFr) for Single and Multiple Clusters	M. Kouril and J.L. Paul (University of Cincinnati, USA)

04:40PM Coffee break

05:00PM Session 11: Applications

Chair: Ingrid Verbauwhede (University of California at Los Angeles, USA)

Approximating the Optimal Replacement Algorithm	B. Juurlink (Delft University of Technology, The Netherlands)
Parallel Simulation of Orography Influence on Large-Scale Atmosphere Motion on APEmille	M. Francia (University of L'Aquila, Italy), E. Panizzi (University of Rome "La Sapienza", Italy), A. Pericola and G. Visconti, (University of L'Aquila, Italy)
A New Technique to Calculate Dipolar Energy and Its Implementation onto an Application Specific Processor	M. Bera, G. Danese, F. Leporati and A. Spelgatti (University of Pavia, Italy)

Repairing Return Address Stack for Buffer Overflow Protection	Y.-J. Park and G. Lee (University of Illinois at Chicago, USA)

06:40PM End of sessions

08:00PM Banquet

Friday, 16 April 2004

08:00AM Registration

08:35AM Session 15 (part A): Processors

Chair: Iliya Georgiev (Metro State College of Denver, USA)

Integrated Temporal and Spatial Scheduling for Extended Operand Clustered VLIW Processors	R. Nagpal and Y. N. Srikant (Indian Institute of Science, India)

09:00AM Session 12: Pipelined Architectures

Chair: Monica Alderighi (CNR, Italy)

MaRS: A Macro-pipelined Reconfigurable System	N. Tabrizi, N. Bagherzadeh, A.H. Kamalizad and H. Du (University of California at Irvine, USA)
Fault Tolerant Clockless Wave Pipeline Design	T. Feng, B.Jin, J.Wang, N.Park (Oklahoma State University, USA), Y.B. Kim and F. Lombardi (Northeastern University, USA)

09:50AM Session 13: Special Session on Reconfigurable Computing (part A)

Organizer and Chair: Juergen Becker (University of Karlsruhe, Germany)

The Digital Divide of Computing	R. Hartenstein (Technical University of Kaiserslautern, Germany)
The Happy Marriage of Architecture and Application in Next-Generation Reconfigurable Systems	I. Verbauwhede and P. Schaumont (University of California at Los Angeles, USA)
Reconfigurable Platforms for Ubiquitous Computing	M. Glesner, T. Hollstein, L. Indrusiak, P. Zipf, T. Pionteck, M. Petrov, H. Zimmer and T. Murgan (Darmstad University of Technology, Germany)

11:00AM Coffee break

11:20AM Session 14: Special Session on Reconfigurable Computing (part B)

Organizer and Chair: Juergen Becker (University of Karlsruhe, Germany)

Physical Design Methodologies for Performance Predictability and Manufacturability	R. Reis (Federal University of Rio Grande do Sul, Brazil), F. Lima Kastensmidt, (State University of Rio Grande do Sul, Brazil) and M. Güentzel (Federal University of Pelotas, Brazil)
Platform-Independent Methodology for Partial Reconfiguration	D. Koch and J. Teich (University of Erlangen-Nuremberg, Germany)
Adaptive Architectures for an OTN Processor: Reducing Design Costs Through Reconfigurability and Multiprocessing	T. Murgan, M. Petrov, M. Majer, P. Zipf, M. Glesner (Darmstadt University of Technology, Germany), U. Heinkel, J. Pleickhardt, B. Bleisteiner (Lucent Technologies, Germany)
Designing and Testing Fault-Tolerant Techniques for SRAM-based FPGAs	F. Lima Kastensmidt (State University of Rio Grande do Sul, Brazil), G. Neuberger, L. Carro and R. Reis (Federal University of Rio Grande do Sul, Brazil)

01:00PM Lunch

02:10PM Session 15 (part B): Processors

Chair: Iliya Georgiev (Metro State College of Denver, USA)

Predictable Performance in SMT Processors	F.J. Cazorla (Technical University of Catalonia, Spain), P.M.W. Knijnenburg (Leiden University, The Netherlands), R. Sakellariou (University Manchester, UK), E. Fernandez (University de las Palmas de GC, Spain), A. Ramirez and M. Valero (Technical University of Catalonia, Spain)
Fault Secureness Need for Next Generation High Performance Microprocessor Design for Testability Structures	C. Metra (University of Bologna, Italy), T.M. Mak (Intel Corporation, USA) and M. Omana (University of Bologna, Italy)
High Performance Code Compression Architecture for the Embedded ARM/THUMB Processor	X.H. Xu, C.T. Clarke (University of Bath, UK) and S. Jones (MediaLab Europe, Ireland)

03:25PM Session 16: Accelerators

Chair: Sergio D'Angelo (CNR, Italy)

Accelerating the Secure Remote Password Protocol Using Reconfigurable Hardware	P. Groen (Delft University of Technology, The Netherlands), P. Hämäläinen (Tampere University of Technology, Finland), B. Juurlink (Delft University of Technology, The Netherlands) and T. Hämäläinen (Tampere University of Technology, Finland)
SoC design of Ogg Vorbis Decoder Using Embedded Processor	A. Kosaka, S. Yamaguchi (Osaka University, Japan), H. Okuhata (Synthesis Corporation, Japan), T. Onoye and I. Shirakawa (Osaka University, Japan)

04:15PM Coffee break

04:35PM Session 17: Architectures

Chair: Kemal Ebcioglu (IBM, USA)

A Perspective on the Future of Massively Parallel Computing: Fine-Grain vs. Coarse-Grain Parallel	P. Tosic (University of Illinois at Urbana-Champaign, USA)
Opportunities and Challenges in Application-Tuned Circuits and Architectures Based on Nanodevices	T. Wang, Z. Qi and C.A. Moritz (University of Massachusetts at Amherst, USA)

05:25PM Closing Remarks

Chair: Stamatis Vassiliadis (Delft University of Technology, The Netherlands)